IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 11, November 2015

Test Validation of MST Radar 3-channel Digital Receiver

T Rajendra Prasad[1,2], K Gayathri[2], T Venkateswarlu[2], P Satyanarayana[2,3]

National Atmospheric Research Laboratory (NARL), Gadanki, India[1]

Sri Venkateswara University College of Engineering, Tirupati, India[2]

Annamacharya Institute of Technology and Sciences, Tirupati, India[3]

Abstract: A 3-channel Digital Receiver is developed for atmospheric science research applications with MST Radar to implement the spaced antenna, Interferometer techniques using spatially distributed antenna modules. The single channel IF digital receiver operational with VHF Mesosphere-Stratosphere-Troposphere (MST) Radar has been upgraded by additional hardware 3-channel backend IF down/up converter module and digital receiver software module test validated at NARL. The 3-channel Digital receiver is attached to MST radar and satisfactory results are obtained. This paper presents the specifications and hardware details of digital receiver, test results with MST Radar, including performance tests with simulated signals. It outlines the Indian MST Radar signal and data processing, method of offline data processing along with the test validation activity of 3-channel digital receiver.

Keywords: Digital receiver, up/down converter, MST radar.

I. INTRODUCTION

The MST technique involves the use of large, coherent radar systems operating in the VHF-UHF range (30-60 MHz) to obtain echoes from the atmosphere in the height range of 1-700 km. The primary echoing mechanism is based on the back scatter from refractive index irregularities having scale size equal to one-half of the radar wavelength.

MST Radar Block Diagram

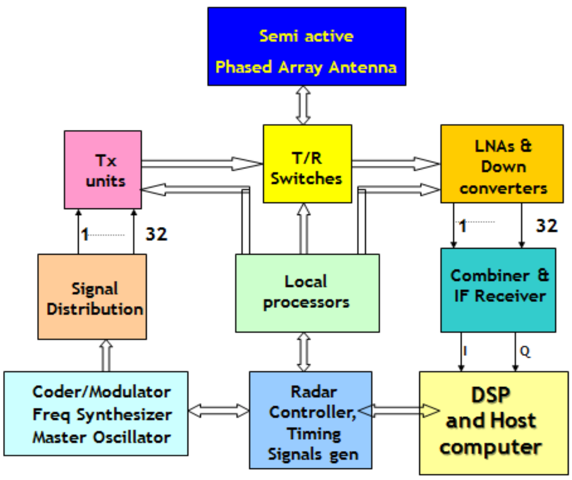

Fig1: MST Radar block diagram

The Doppler Beam Swinging (DBS) technique is used for obtaining atmospheric parameters at present at Indian MST Radar. In this method a single channel receiver is sufficient, and beam steering is used to obtain echoes from different directions of the atmosphere. A three dimensional wind vector is obtained above the antenna system by three axes (i.e. x, y, z components of winds). The assumption of homogeneity during the time period of antenna beam steering, which is about 3 minutes is limitation of this method. This assumption of homogeneous back ground wind condition fails during cyclonic and thunderstorm conditions. Other techniques like spaced antenna and interferometer are used during these extreme wind conditions. These techniques need multiple antennas and independent receiver systems to record data. So, the existing single channel digital receiver is being upgraded and test validated to function as three channels in this exercise.

MST Radar System description:

The four important basic radar subsystems are Antenna array and feeder network, Exciter and Radar controller, Transmitter system, Receiver and Signal processing.

Antenna array and feeder network

The radar consists of two planar phased antenna arrays with of 1024 three element Yagi-Uda antennas each. Linear horizontal polarization is used in both arrays, with dipoles oriented in east-west direction in one array and in north-south direction in another array. The antenna elements are collocated on 1024 poles arranged in a 32X32 matrix over an area of 130mX130m. It generates a radiation pattern with a main lobe of 3^0 and a gain of 36 dB. The inter-element spacing in the matrix grid is 0.7λ, where λ is radar wavelength. Modified Taylor distribution was adopted for the aperture a first side lobe level of -20dB are realized. The antenna pattern has been characterized in the receive mode by recording the radio source Virgo-A (3C274) using the phase switching interferometer technique of *Ryle*, 1952.

Exciter and Radar controller

The exciter unit generates all the RF and timing and control signals for various subsystems of the radar. The 5 MHz RF synthesizer is a highly stable reference signal generator. The 48 MHz synthesizer serves as local oscillator (LO) for up-conversion at the time of transmitting and down-conversion while receiving. The Transmitter bi-phase coder generates a 5 MHz complementary coded RF pulse and the simulate coder generates 53 MHz complementary coded RF pulse with a given Doppler shift and range delay to provide as a simulation test signal. Simulated signal is used for verification of the receiver and signal processor performance. The distributed radar controller with 8085-microprocessor and RS232 based systems are upgraded with optical fibre LAN and CPLD/ FPGA based systems for electronic beam steering and time synchronized automated experiments execution.

The timing and control signal generator (TCSG), a programmable multi channel pulse generator supplies control signals for synchronizing the operations of various subsystems of the radar. TCSG design is based on ADSP 21062 SHARC DSP processor operating. The first 28 bits of 48-bit data bus are used for generation of control signals by bit length encoding method. The outputs from TCSG include transmitter and receiver gate signals, duplexer signal, coder and analog-to-digital converter (ADC) sample clocks.

Transmitter system

The transmitter system consists of 32 transmitters ranging in power from 15 kW to 120 kW to provide a total transmitter power of 2.5 Mega watts. High power transmitters feed the central area and low power ones feed peripheral antennas for better antenna side lobe level. Each transmitter has four amplifying stages and related power monitoring and controlling and safety interlock circuits. The input to the transmitter is 1milli watt pulse-modulated (coded / un-coded) signal at 53 MHz.

The output power of the transmitter has to be maintained within ± 1 dB of the specified level by adjusting the input to SSA by means of a PIN attenuator, by sensing transmitter output power level in –60dB dual directional coupler (RF power-monitor coupler). The radar controller remotely controls the transmitter power on off sequence and monitors the safety health parameters with the help of four local processors serving a group of eight transmitters. The local processor also buffers the control signals to duplexers, polarization switches and Receiver Blanking switches along with the main task of providing digital phase shifter data for 8 bit phase shifters.

Receiver and Signal processing

The receiver is a phase coherent receiver with quadrature channels, having an overall gain of 120dB, a dynamic range of 70dB, and a bandwidth matched to the baud length of the coded pulse. The signal processor FEPU accepts two analog inputs I and Q from radar receiver, two synchronizing clocks called base clock and IPP marker. The ADSP 21060 SHARC processor controls the operations of the FEPU at the clock speed of 40MHz. ADC 9240 a 14 bit analog-to-digital converter with dynamic range 85 dB and sampling frequency of 1 MHz is used for digitizing the I and Q after buffering in video amplifier and offset to nonnegative voltage.

The digital data is sign extended to 32 bit twos complement integer representation. The high-speed hardware digital transversal filter IC, IMS A 100, performs the decoder function. The decoder output is transferred to main memory by the dual buffer mode for coherent integration and further processing in the host computer and finally to the data archival system.

Table 1**:** Radar specifications

Serial number	Parameter	MST Radar
1.	Operating frequency	53MHz
2.	IF Frequency	5MHz
3.	Range resolution	150m
4.	Maximum height of observation	20km for wind, 800 km for Ionosphere studies
5.	Wind velocity resolution	0.1m/sec (typical)
6.	Mode of wind extraction	Doppler beam swinging method
7.	Pulse compression code length	16 bit (typical)
8.	Coherent integration length	4, 8, 16, 32, 64, 128, 256 (typical)
9.	Fast Fourier Transform (FFT)	32, 64, 128, 256, 512, 1024 (typical)

II. DIGITAL RECEIVER

A digital receiver was implemented for VHF radar IF signal processing recently utilising latest DSP processor. The main advantage of digital receiver is its programmability and upgrades to the system by software code redesign. The digital receiver features decimation and filtering to reduce the sampling rate, decoding for coded transmission, coherent integration, dc removal, windowing, FFT / power spectrum computation, incoherent integration, estimation of moments, UVW, wind speed and direction, data transfer to host computer with proper data format for archival and display. The block diagram of digital receiver was shown below in figure 2.

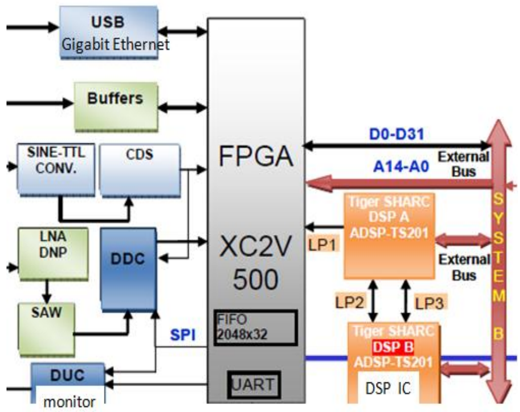

Fig: 2 Digital receiver block diagram

 DOI 10.17148/IJARCCE.2015.411121

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 11, November 2015

Figure2 represents the functional block diagram of Digital receiver. The radar receiver IF signal is processed by Digital receiver IF filter and gain modules LNA, digitally variable gain amplifier. ADC DDC chip AD6654 performs digital down conversion function of IF to Baseband super heterodyne receiver. ADSP TS201 performs signal processing functions and FFT. FPGA is used for buffering the data between DDC and DSP as well as to generate necessary timing and control signals and coherent integration. The processed data is transferred to host computer by USB 2.0 interface.

Digital receiver salient features and signal processing functions consists of

a) Input analog frequency ranging 0-70 MHz,
b) 5 MHz bandwidth to facilitate the direct digitization of radar receive RF (53MHz) / IF signals (5MHz),
c) 14-bit ADC realizing 75-dB dynamic range,
d) Digital domain down conversion completely eliminates the errors due to phase and amplitude imbalances,
e) Automatic selection of digital filter bandwidth corresponding to baud length, for matched filter response,
f) Time domain DC removal and coherent integration,
g) Power spectrum computation with complex Fast Fourier Transformation and incoherent averaging.

Figure 3 represents the functional block diagram of the AD6654, a mixed IF signal to base band receiver consisting of a 14-bit, 92.16 MSPS analog to digital converter (ADC) and 6 channel DDC capabilities. The AD6654 is used as part of radio systems that digitally demodulates and filters IF sampled signals. It has three 16-bit parallel output ports and Tiger SHARC compatible 8/16- bit microprocessor port. This multiple channel DDC capability is exploited to extend the single input digital receiver to multiple input digital receiver with the addition of an IF module to multiplex the three antenna signals and separate the three antennas digital data using software in Digital receiver.

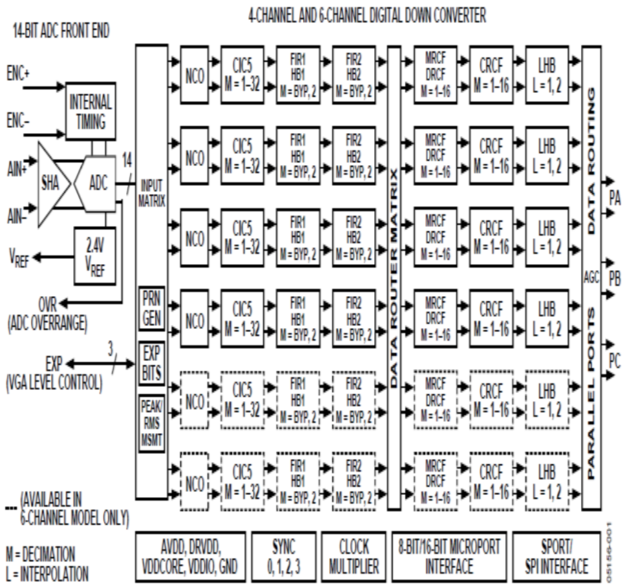

Fig3: AD6654 block diagram

III. HARDWARE MODULE OF THREE CHANNEL DIGITAL RECEIVER

Figure 4 represents the RF module for the enhancement of the single digital receiver with three channel input system. The RF module consists of 3 inputs, one each for three IF signals at 5MHz frequency, two analog mixers to up /down convert IF of 2nd antenna to 3 MHz, 3rd antenna to 7 MHz using an internal local oscillator module of 2 MHz, and an RF 3:1 power combiner to feed the module output to Digital Receiver.

The Digital Receiver hardware has been upgraded with installation of 2nd DSP chip, gigabit Ethernet card and timing and control signals buffer circuits. The software and firmware are modified for the functionality requirement of three channel signal processing and data archival. The programmable NCOs of the digital receivers are set to the corresponding IF for baseband data extraction.

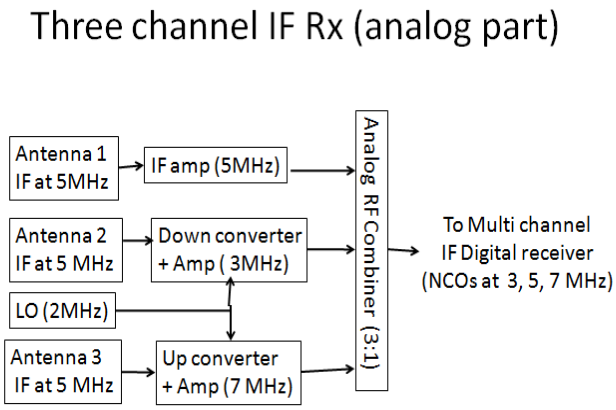

Fig 4: Three channel backend IF module.

The staggered Inter pulse period/ multiple IPP are programmed in the three channel digital receiver for ionospheric studies and pulse to pulse beam steering, (if, necessary). The set of parameters upgraded in the three channel digital receiver are shown in Table 2.

Three channel digital receiver experimental parameters are tabulated as follows for the testing with simulate signals using three signal generators giving 3, 5, 7 MHz along with known dopplershift and pulse delay of known time. The respective 3d plots observed are as follows.

Table2: Digital receiver parameters

Parameters	**Value**
Mode of operation	Coded
Code length	8 bit code
Baud length	1µsec
Pulse width	8µsec
IPP on time	1 µsec
Coherent integration length (NCI)	64
Number of range bins (NRGB)	40
Fast Fourier Transform (NFFT)	256
DVGA gain code	0X88 (28 dB)

 DOI 10.17148/IJARCCE.2015.411121

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 11, November 2015

Input level	-50dBm
Number of sub IPPs	1(multi channel)
Sub IP time	160µsec
CH1 NCO Frequency	**3 MHz**
CH2 NCO Frequency	**5 MHz**
CH3 NCO Frequency	**7 MHz**

IV. 3-CHANNEL DIGITAL RECEIVER TESTING RESULTS

The test validation of the hardware and software of three channel digital receiver is performed by simulating the pulsed IF signal with known frequency shift and known timed delay by a signal generator operating at 5MHz. The shift in IF signal-frequency is represented in the digital receiver output at expected frequency and range corresponding to time delay. Figure 5 represents the simulated signal time domain plot at 10th range bin, representing 5 Hz frequency shift in 5MHz IF frequency in the digital receiver recorded data for channel 1. Top panels are providing I channel data and bottom panels shows the Q channel data of real time recorded times-series data with three channel receiver. Note, X-axis represents time and Y-axis represents range bin data at corresponding height/range.

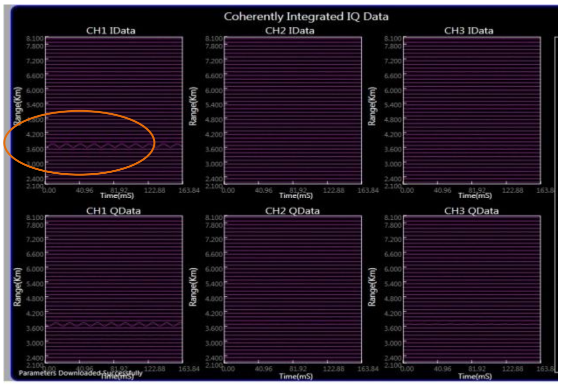

Fig 5: Time Domain plot of channel-1 data

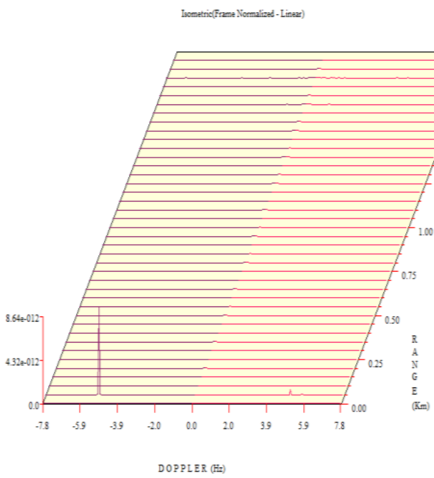

Figure6: 3D plot of channel-1 data (NCO-3MHz)

The stored output of the digital receiver is processed using the Atmospheric Data processor (ADP) software. Figure 6 represents the spectral domain three dimensional (3D) plot of another simulate signal test result. The signal peak is present at - 5 Hz Doppler frequency in the first range bin; we may observe the little amount of image signal at +5Hz frequency in the first range data plot. This implies that the image rejection is better than -20 dB, when compared in amplitude levels. The digital down conversion is successfully tested for amplitude imbalances of the I and Q channel amplitudes.

Figure 7 represents the 3d power spectrum plot of channel 2 data (NCO 5MHz) representing +5 Hz frequency shift in 5MHz IF frequency at 1st range bin.

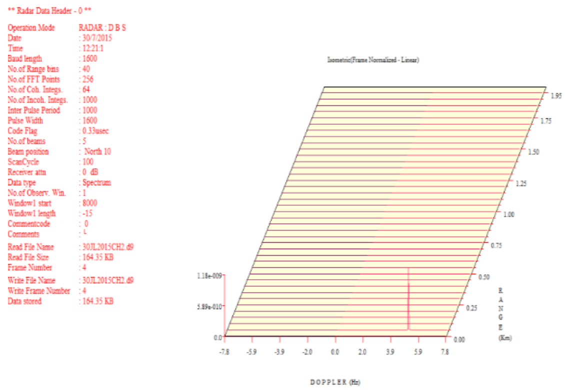

Fig 7: 3D plot of channel-2 data (NCO-5MHz)

The operating parameters are 16 µs coded, pulse with 1 µs baud length, 1000 µs inter pulse period, 64-numbers of coherent integrations (NCI), 256 FFT points, for 5 beams and 40 range bins(NRGB). The beam position is at north 10 and the number of scan cycles are 100. X-axis represents Doppler frequency; Y-axis represents range bin data and Z axis represent the amplitude of the simulated signal at corresponding height/range.

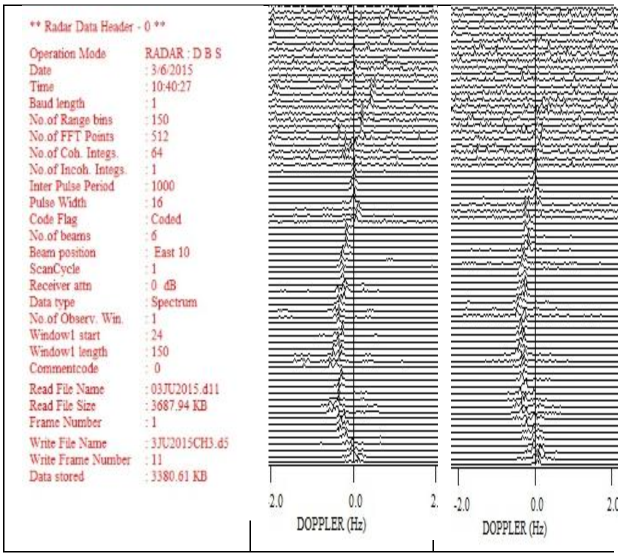

Fig 9: Comparison of 2d spectral plot of Single channel digital receiver and three-channel digital receiver, when both connected to MST Radar system parallel.

Figure 9 represents the comparision of 2d spectral plot of single channel digital receiver and three channel digital receiver is when connected to MST radar (first resuts). Both the receiver are showing similar profile of the data up to 12km. The header of the experiment data with operating parameters is also shown in the figure in first column. The beam position is at East 10. Here X-axis represents Doppler frequency; Y-axis represents range bin data.

V.CONCLUSION

The 3-channel digital receiver functionality and performance are quite satisfactory as the signal detectability is tested with simulate signals and atmospheric data record on sample basis. The matching of derived spectral parameters is obtained in comparison plots. The end to end functionality of IF signals to atmospheric parameters extraction is performed successfully with 3-channel digital receiver. For multi-receiver requirement of spaced antenna and imaging applications of active array MST Radar system, this 3-channel digital can be used.

REFERENCES

[1] Introduction to Radar Systems- Merill I. Skolnik, TMH Special Indian Edition, 2nd Edition, 2007.
[2] Radar Principles- Peebles, Jr., P.Z.Wiley, NewYork, 1998.
[3] Radar Principals, Technology, Applications – Byrron Edde, Pearson Education, 2004
[4]. Anandan V.K., Atmospheric Data Processor-Technical and User reference manual, National Atmospheric Research Laboratory, Gadanki.
[5]. Rabiner L.R., and B.Gold, Theory and applications of Digital Signal Processing, Prentice Hall, Englewood Cliffs,N.J,1975.

ACKNOWLEDGMENTS

The authors thank the staff and authorities of Sri Venkateswara University College of Engineering (SVUCE), National Atmospheric Research Laboratory (NARL) for extending the support in all respects during the project tenure.

BIOGRAPHIES

Thommundru Rajendra Prasad has received ECE Diploma (1988), B.E (2000), M. Tech (2006) and currently pursuing Ph.D. at Sri Venkateswara University, Tirupati, AP, India. He is with Society for Applied Microwave Electronics Engineering Research (SAMEER), Department of Electronics, Govt. of India, Mumbai, during installation of MST Radar (91-94). He joined National Atmospheric Research Laboratory, Department of Space, Government of India during 1994 and since then, he is involved in state-of-the-art technological developments of the VHF phased array radar. His research interest is signal processing.

Kandala Gayathri completed her B.Tech in Electronics & Communication Engineering at Siddhartha Institute of Engineering and Technology, Puttur, Affiliation to JNTUA, Anantapuram, INDIA in 2012. She is pursuing her M.Tech Degree with specialization in Signal Processing (SP) at SVUCE, SV University, Tirupati, INDIA. Her areas of interest include Signal Processing and CommunicationSystem.

T Venkateshwarulu received B.Tech degree in Electronics and Communication Engineering and M.Tech degree in Instrumentation & Control Systems and obtained Ph.D. from Sri Venkateswara University, Tirupati in 1992, 1995, and 2013 respectively. He is a member in ISTE, IE, and BMSI. Currently, he is working as Associate Professor in the Department of Electronics and Communication Engineering, Sri Venkateswara University, Tirupati, Andhra Pradesh, India.

P Sathyanarayana has received B.Tech (E.C.E, 1976), M.Tech (Instrumentation & Control systems, 1978) and Ph.D. (Digital Signal Processing, 1987) from S.V. University Tirupati. He worked as Post Doctoral Fellow in 1-D and 2- D Signal Processing in Dept of Electrical and Computer Engg., Concordia University, Montreal, Canada from 1988-1990. He was with Sri Venkateswara University College of Engineering, Tirupati, India. He is now with Annamacharya Institute of Technology and Sciences, Tirupati, India. He worked as Head, Dept. of E.E.E, S.V. University, Tirupati, A.P., India. He indeed visited many countries like Malaysia, U.S.A and other countries as visiting faculty. He was the principal investigator for DST sponsored project. He presented 16 papers in International Journals like IEEE & IETE.